

What is claimed is:

1 1. A dual chips stacked packaging structure,
2 comprising:

3 a first chip, having an active surface and an
4 opposing non-active surface, the active surface
5 consisting of a central area and a peripheral
6 area having a plurality of first bonding pads;

7 a lead frame, comprising a plurality of leads and a
8 chip paddle having a first adhering surface and
9 a second adhering surface, the first adhering
10 surface adhered to the active surface of the
11 first chip in such a way as to avoid contact
12 with the first bonding pads;

13 a second chip, having an active surface and an
14 opposing non-active surface connecting with the
15 second adhering surface of the chip paddle, the
16 active surface consisting of a central area and
17 a peripheral area having a plurality of second
18 bonding pads; and

19 a plurality of wires, wherein parts of the wires
20 electrically connect with the first bonding pad
21 and the leads, and parts of the wires
22 electrically connect with the second bonding
23 pad and the leads.

1 2. The structure as claimed in claim 1, wherein
2 the first adhering surface of the chip paddle and the
3 active surface of the first chip are adhered by a non-
4 conductive solid or liquid adhesive.

1 3. The structure as claimed in claim 1, wherein
2 the second adhering surface of the chip paddle and the
3 non-active surface of the second chip are connected by a
4 solid or liquid adhesive.

1 4. The structure as claimed in claim 1, wherein
2 the wires are metal lines.

1 5. A dual chips stacked packaging structure,
2 comprising:

3 a first chip, having an active surface and an
4 opposing non-active surface, wherein the active
5 surface consists of a central area and a
6 peripheral area having a plurality of first
7 bonding pads;

8 a lead frame comprising a plurality of leads and a
9 chip paddle having a first adhering surface and
10 a second adhering surface, the first adhering
11 surface adhered to the active surface of the
12 first chip in such a way as to avoid contact
13 with the first bonding pads;

14 a second chip, having an active surface and an
15 opposing non-active surface connecting with the
16 second adhering surface of the chip paddle,
17 wherein the active surface consists of a
18 central area and a peripheral area having a
19 plurality of second bonding pads;

20 a plurality of wires, parts of which electrically
21 connect with the first bonding pad and the

22 leads, and parts of which electrically connect
23 with the second bonding pad and the leads; and
24 an encapsulation, covering the lead frame, the first
25 chip, the second chip, and the wires.

1 6. The structure as claimed in claim 5, wherein
2 each lead further comprises an inner lead covered by the
3 encapsulation and outer lead extending beyond the
4 encapsulation.

1 7. The structure as claimed in claim 5, wherein
2 the first adhering surface of the chip paddle and the
3 active surface of the first chip are adhered by a non-
4 conductive solid or liquid adhesive.

1 8. The structure as claimed in claim 5, wherein
2 the second adhering surface of the chip paddle and the
3 non-active surface of the second chip are connected by a
4 solid or liquid adhesive.

1 9. The structure as claimed in claim 5, wherein
2 the wires are metal lines.

1 10. A dual chips stacked packaging structure,
2 comprising:

3 a first chip, having an active surface and an
4 opposing non-active surface, wherein the active
5 surface consists of a central area and a
6 peripheral area having a plurality of first
7 bonding pads;

8 a lead frame, comprising a plurality of leads and a
9 chip paddle having a first adhering surface and

10 a second adhering surface, the first adhering
11 surface adhered to the active surface of the
12 first chip in such a way as to avoid contact
13 with the first bonding pads, and each of the
14 leads comprising a wire connecting surface and
15 a wire non-connecting surface;

16 a second chip, having an active surface and an
17 opposing non-active surface connecting with the
18 second adhering surface of the chip paddle,
19 wherein the active surface consists of a
20 central area and a peripheral area having a
21 plurality of second bonding pads;

22 a plurality of wires, parts of which electrically
23 connect with the first bonding pad and the
24 leads, and parts which of electrically connect
25 with the second bonding pad and the leads; and

26 an encapsulation, covering the chip paddle, the
27 second chip, the wire connecting surface of the
28 leads, the active surface of the first chip,
29 and the wires, with the non-active surface of
30 the first chip and the wire non-connecting
31 surface of the leads exposed beyond the
32 encapsulation.

1 11. The structure as claimed in claim 10, wherein
2 each lead further comprises an inner lead covered by the
3 encapsulation and outer lead extending beyond the
4 encapsulation.

1 12. The structure as claimed in claim 10, wherein
2 the first adhering surface of the chip paddle and the

3 active surface of the first chip are adhered by a non-
4 conductive solid or liquid adhesive.

1 13. The structure as claimed in claim 10, wherein
2 the second adhering surface of the chip paddle and the
3 non-active surface of the second chip are connected by a
4 solid or liquid adhesive.

1 14. The structure as claimed in claim 10, wherein
2 the wires are metal lines.